REMARKS/ARGUMENTS

Claims 1-7, 10-15, 44, and 46-54 were pending in the application. Upon entry of this amendment amending claims 1, 44, and 51, claims 1-7, 10-15, 44, and 46-54 remain pending. Under 35 U.S.C. §103(a) claims 1-2, 4-5, and 7, and 10-14 stand rejected as being unpatentable over U.S. Patent No. 5,479,618 issued to Van de Steeg et al. (hereinafter "Steeg"), in view of U.S. Patent No. 6,414,368 issued to May et al. (hereinafter "May"), in view of U.S. Patent No. 4,796,211 issued to Yokouchi et al. (hereinafter "Yokouchi"), claim 3 stands rejected over May, Yokouchi , and Steeg, in view of U.S. Patent No. 6,5050,341 issued to Harris et al. (hereinafter "Harris"), claim 6 and 15 stand rejected over May, Yokouchi , and Steeg, in view of U.S. Patent No. 5,721,828 issued to Frisch (hereinafter "Frisch"), claims 44, 46-51, and 53 stand rejected over Yokouchi in view of Steeg, and May, claim 52 stands rejected over Yokouchi in view of Steeg, in further view of U.S. Patent No. 6,298,360 issued to Muller (hereinafter "Muller"). Claim 54 stands rejected over Yokouchi in view of Steeg, in further view of U.S. Patent No. 6,754,830 issued to Laiho et al. (hereinafter "Laiho").

Applicants submit a request for continued examination herewith to allow entry of this amendment.

Applicants aver that no new matter has been added in this response.

Examiner Interview

Applicants appreciate the interview with the Examiner on October 24, 2006, where claim amendments and the cited art were discussed in general.

§103 Rejections

Claims 1 and 44

Claims 1 and 44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Steeg, Yokouchi, May, Frisch, Muller, and Laiho. But these references do not show or suggest each and every element of claim 1 and claim 44. For example, claim 1 as amended partially recites "periodically reloading [a] count register with [an] initial value, wherein the reloading is caused by receiving a first magic value, wherein the first magic value when received configures the watchdog timer circuit to respond to a second magic value that is different from the first magic value, wherein the second magic value when received configures the watchdog timer circuit to respond to a third magic value that is different from the second magic value", and claim 44 as amended partially recites "loading a first magic value into a reload register that is a part of [a] watchdog timer circuit, which resets [a] count register to an initial value, wherein the first magic value when loaded configures the watchdog timer circuit to respond to a second magic value that is different from the first magic value, wherein the second magic value when loaded into the reload register configures the watchdog timer circuit to respond to a third magic value that is different from the second magic value". The cited references do not provide this combination of features.

In the Office Action, the Examiner states that Steeg provides each of the recited features and states that May discloses a method of operating a programmable logic circuit having a watchdog timer integrated on the same die, and states that Yokouchi discloses the operation of the watchdog timer using a first magic value that configures the watchdog timer to respond to a second magic value, where Harris discloses an external source that is a serial EPROM, and that Frisch discloses a timer circuit which decrements a stored count value pointing to columns 3, 6, 8-9 and Figure 4 *et seq.* of Steeg, column 40-43 *et seq.* of May, column 1 *et seq.* of Yokouchi, figure 2 and column 9 *et seq.* of Harris, and columns 27-28 *et seq.* of Frisch.

In addition, the Examiner stated in the Office Action with regard to claim 44, Yokouchi discloses clocking a watchdog timer circuit on the programmable logic circuit, loading a first magic value, loading a second magic value into the reload register which causes the

watchdog timer circuit to generate a triggered signal, Steeg discloses receiving the triggered signal in a reset logic block which causes a reloading of configuration data from an external source, May discloses a method of operating a programmable logic circuit having a watchdog timer integrated on the same die, Muller discloses a final value that is user selectable, and that Laiho discloses that in a debug mode the counter does not advance pointing to column 1 *et seq.* of Yokouchi, columns 3, and 8-9 figure 2, and 4-5 *et seq.* of Steeg, column 40-43 *et seq.* of May, figure 2 and column 6 *et seq.* of Muller, and column 4 *et seq.* of Laiho. The Applicants respectfully traverse these rejections.

Steeg discloses placing a watchdog timer on a first programmable logic circuit 29, and the reloading of configuration data on a second programmable logic circuit 37. The first programmable logic circuit and the second programmable logic circuit are physically and electrically isolated to prevent faults and other noise associated with the second programmable logic circuit from affecting the first programmable logic circuit. As taught by Steeg, without electrical isolation, circuit interruptions and power losses from the second programmable logic circuit (e.g., the I/O circuit) could damage or disable the watchdog timer circuit (e.g., the controller electronics) (See Steeg, Figures 4 and 5, col. 1 lines 32-37, and col. 8, lines 49-59). As Steeg requires physical and electrical isolation, Steeg teaches away from placing a watchdog timer and reloading register on the same die. Therefore, it is not obvious when referring to Steeg to place the first and second programmable logic circuit on the same die as claimed.

Yokouchi discloses at column 1 lines 36-60:

> "The watchdog timer described in the literature (2) comprises a 16-bit up-counter that prevents the CPU from running out of control. The watchdog timer is initialized by writing the data 1EH to it. Next the 1's complement of 1EH, which is OE1H, is written to enable the counter, which commences free-run counting. During operation, if the 1EH and 0E1H data are successively written to the watchdog timer within 16ms (at 12 MHz), the watchdog timer

resets and starts counting again from 0. To reset the watchdog timer, in other words, a combination of fixed data must be written in succession to the watchdog timer within a fixed time.

If the combination of the data to reset the watchdog timer is not written within the fixed time, the watchdog timer generates a carry signal. The carry signal resets the CPU, causing it to restart program execution from address O. This prevents "runaway" of the CPU, i.e., prevents the CPU from continuing to execute a program that has gone out of control.

A problem with the above watchdog timers is their inability to prevent program runaway accurately. This is because there is a certain probability that a runaway program resets the watchdog timer by writing the data identical (by chance) to those defined for resetting, so that the runaway is not detected (emphasis added)."

In other words, Yokouchi discloses a problem with the prior art which teaches writing two static values within a specified time in order for the reset to occur, which can cause runaway conditions under certain circumstances. Yokouchi is therefore improperly combinable with the other cited references. Even if combinable, to overcome the problems listed above with the prior art, Yokouchi discloses a watchdog timer circuit that is completely different from the claimed subject matter. For example, Yokouchi discloses employing two counters. The first counter 53 outputs an overflow (carry) signal F when it overflows. The second counter 32 counts the number of times the first counter has been reset. A reset value A is written to latch 31 and compared to the output value B of the second counter via comparator 33. When the reset value and the number of times the first counter resets match (A=B), the comparator outputs a reset signal C, the first counter is reset via a reset signal E derived from the reset signal C. In order for the resets to continue, a new reset value A, greater in value than the initial reset value A, must be written to latch 31 so that the second counter can continue incrementing before the

next reset signal E is asserted. If the next reset value A is not written to latch 31, the first counter 53 overflows and asserts signal F.

May does not discloses a watchdog timer circuit, but discloses a microcomputer having high-density RAM on a single die. Muller discloses a method for generating a random number, and Frisch discloses a multi-computer memory access architecture using a crossbar network to connect processing nodes. Harris discloses a serial EPROM used for storing configuration data, and Laiho discloses a method to prevent the unauthorized use of a protected interface of a processor where an authorized debugging user uses an infrared transmitter to transmit a secret code word that stops the co-processor from incrementing or decrementing, or disables the issuance of reset and standby signals. Applicants submit that May, Muller, Frisch, and Laiho do not make up for what Yokouchi and Steeg lack.

Therefore, Yokouchi, Steeg, May, Frisch, Muller, and Laiho alone or in combination do not disclose *a first magic value when loaded configures the watchdog timer circuit to respond to a second magic value that is different from the first magic value, and when the second magic value is loaded, the watchdog timer circuit is configured to respond to a third magic value that is different from the second magic value* as claimed (emphasis added). On the contrary, the watchdog timer as disclosed by Yokouchi, even if combinable with the other cited references, only asserts the reset signal C when value A initially latched into latch 31 and the value B output of the second counter 32 *are the same value* (e.g., *A=B*) (Emphasis added) (See Yokouchi, Figure 1, col. 4, line 1, through col. 6, line 65).

Therefore, Applicants submit that claim 1 and claim 44 are patentably distinguished over the cited references, alone or in combination.

Claims 1-7, 10-15, and 46-54

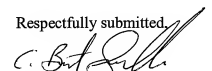
Claims 1-7 and 10-15 depend from claim 1, and claims 46-54 depend from claim 44 and are therefore allowable for at least the reasons discussed in relation to claims 1 and 44, as well as the limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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